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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,335	10/19/2001	Shuichi Takayama	NAK1-BG86b	9991

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EXAMINER	
RAMPURIA, SATISH	
ART UNIT	PAPER NUMBER
2191	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/051,335	TAKAYAMA ET AL.	
	Examiner	Art Unit	
	Satish S. Rampuria	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *49-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *49-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/24/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the RCE filed on Aug 24, 2005.

2. Claims cancelled by the Applicants: 1-48

3. New claims added by the Applicant: 49-53

4. Claims 49-53 are pending.

5. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/24/2005 has been entered.

Information Disclosure Statement

6. An initialed and dated copy of Applicant's IDS form 1449 filed on 8/24/2005 is attached to the instant Office action.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the **second paragraph** of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 49 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Clarification and/or correction are required.

Regarding claim 49, the limitation, "boundary information" is unclear as to what is the boundary information, is it size of the instructions or something in that nature.

The rejection of the base claim 49 is necessarily incorporated into the dependent claims 50-53.

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 31-35 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 2 of U. S. Patent No. 6,834,336 (hereinafter called '336). Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following observation.

Instant Claim	*'336 Claim*
49. (New) A processor that executes instructions converted by a compiler, comprising:	1. A VLIW (Very Long Instruction Word) processor comprising:
a fetching unit configured to fetch instruction packets one by one, wherein each instruction packet has fixed bit length and includes a plurality of instructions, **wherein each instruction has a boundary information bit, a value of which indicates whether the instructionshould be processed together with a succeeding instruction**; and	**a fetching unit configured to fetch the instruction block**, the instruction block including (a) a format field having a format code and (b) an operation field having a code to be processed by the processor, **wherein the format code in the format field indicates whether a code in an operation field of the instruction block should be processed together with a code in the operation field of a succeeding instruction block**; a decoding/judging unit configured to decode the format code of a first instruction block and judge whether to process a first code contained in the operation field of the first instruction block together with a second code contained in the operation field of a second instruction block that succeeds the first instruction block; and **an executing unit configured to process**
an execution unit configured to process an	

instruction contained in a certain instruction packet and another instruction contained in a succeeding instruction packet in parallel based on the value of the boundary information bit, wherein at least one of the instruction packets includes instructions which are processed sequentially, and wherein the value of the boundary information bit is determined by the compiler during static parallel scheduling.	**the first and second codes simultaneously when the decoding/judging unit judges positively, wherein the fetching unit fetches the first instruction block and second instruction block sequentially**.
50. (New) The processor of claim 49, **wherein the execution unit is further operable to process the instruction contained in the certain instruction packet and the another instruction contained in the succeeding instruction packet sequentially based on the boundary information**.	2. The VLIW processor of claim 1, **wherein the executing unit is further operable to process the first code and the second code sequentially when the decoding/judging unit judges negatively**.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 49-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,881,260 to Raje et al. (hereinafter, Raje) in view of US Patent No. 5,226,131 to Grafe et al. (hereinafter, Grafe).

Per claims 49:

Raje disclose:

- A processor that executes instructions converted by a compiler, comprising:a fetching unit configured to fetch instruction packets one by one (col. 3, lines 12-13 "fetch another line of compressed instructions from an instruction cache"), wherein each instruction packet has fixed bit length and includes a plurality of instructions, wherein each instruction has a boundary information bit (col. 5, lines 20-25 "the instruction boundary marker... bit in each word of the instruction format is designated as the start bit... the start bit="1".. designates the start of a new instruction.. the start bit="0"... indicates that this word is a continuation of the current instruction" and FIG. 2 and related discussion), a value of which indicates whether the instruction should be processed together with a succeeding instruction (col. 5, lines 20-25 "the instruction boundary marker... bit in each word of the instruction format is designated as the start bit... the start bit="1".. designates

the start of a new instruction.. the start bit="0"... indicates that this word is a continuation of the current instruction" and FIG. 2 and related discussion); and

- an execution unit configured to process an instruction contained in a certain instruction packet and another instruction contained in a succeeding instruction packet in parallel based on the value of the boundary information bit (col. 5, lines 54-58 "FIG. 3 illustrates the operation of the NEXTPC logic 250 in calculating the program counter values in parallel with decompression of instructions and fetching of additional ICACHE lines when the instruction sequence crosses an ICACHE line boundary"),
- wherein at least one of the instruction packets includes instructions which are processed sequentially (col. 3, lines 25-26 "an instruction sequencing circuit configured to receive the instruction boundary markers"), and
- wherein the value of the boundary information bit is determined (col. 5, lines 20-23 "FIG. 2 uses start bits as the instruction boundary marker.. the start bit="1", this designates the start of a new instruction").

Raje does not explicitly disclose static parallel scheduling.

However, Grafe discloses in an analogous computer system static parallel scheduling (col. 1, lines 30-31 "static direction of parallel execution can be very efficient... system should statically schedule finer grains to pay the synchronization...").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of static parallel scheduling as taught by Grafe into the method of sequencing and decoding variable length instructions with an

instruction boundary marker within each instruction as taught by Raje. The modification would be obvious because of one of ordinary skill in the art would be motivated to use static parallel scheduling to provide an efficiently execution of programs exploiting the maximum amount of parallelism as suggested by Grafe (col. 1, lines 25-29).

Per claims 50:

The rejection of claim 49 is incorporated, and further, Raje disclose:

- wherein the execution unit is further operable to process the instruction contained in the certain instruction packet and the another instruction contained in the succeeding instruction packet sequentially based on the boundary information (col. 5, lines 20-25 "the instruction boundary marker... bit in each word of the instruction format is designated as the start bit... the start bit="1".. designates the start of a new instruction.. the start bit="0"... indicates that this word is a continuation of the current instruction" and FIG. 2 and related discussion and col. 3, lines 25-26 "an instruction sequencing circuit configured to receive the instruction boundary markers").

Per claims 51:

The rejection of claim 49 is incorporated, and further, Raje disclose:

- wherein the processor is capable of executing a variable number of instructions in parallel (col. 3, lines 21-25 "The instruction decoding circuit comprises an instruction buffer configured to receive and store a line of variable length instructions from an instruction cache").

Per claims 52:

The rejection of claim 51 is incorporated, and further, Raje disclose:

- wherein a bit length of instructions which the processor executes in parallel is variable (col. 3, lines 21-25 "The instruction decoding circuit comprises an instruction buffer configured to receive and store a line of variable length instructions from an instruction cache").

Per claims 53:

The rejection of claim 49 is incorporated, and further, Raje disclose:

- an instruction buffer for temporally storing instructions so as to be executed in a later cycle (col. 3, lines 24-29 "The instruction decoding circuit comprises an instruction buffer configured to receive and store a line of variable length instructions from an instruction cache").

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Satish S. Rampuria** whose telephone number is **(571) 272-3732**. The examiner can normally be reached on **8:30 am to 5:00 pm** Monday to Friday except every

other Friday and federal holidays. Any inquiry of a general nature or relating to the status of this application should be directed to the **TC 2100 Group receptionist: 571-272-2100**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Wei Y. Zhen** can be reached on **(571) 272-3708**. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Satish S. Rampuria
Patent Examiner/Software Engineer
Art Unit 2191
11/14/2005

WEI Y. ZHEN
PRIMARY EXAMINER